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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,223	09/28/2001	Chee How Lim	219.40230X00	3861
7590	07/12/2006		EXAMINER	
Edwin H. Taylor BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 12400 Wilshire Boulevard, Seventh Floor Los Angeles, CA 90025			CHEN, TSE W	
			ART UNIT	PAPER NUMBER
			2116	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/965,223	LIM ET AL.	
	Examiner Tse Chen	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 19 May 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 19, 2006 has been entered.

2. Claims 1-20 are presented for examination.

### ***Claim Objections***

3. Claims 1 and 2 are objected to because of the following informalities:

- As per claim 1, “onto an interconnect” should be “onto a first interconnect”; and “from an interconnect” should be “from a second interconnect”.
- As per claim 9, “timing of said received output signal at least one output signal meeting” should be “timing of said received output clock signal or at least one output signal meeting”.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sevalia et al., US Patent 6356122, hereinafter Sevalia.
6. In re claim 1, Sevalia discloses a timing circuit [fig.2; col.1, ll.65-66] comprising:
  - At least one driving circuit [output driver] outputting an output signal onto a first interconnect [associated with output driver] [fig.2].
  - At least one receiving circuit [feedback control switch] receiving an input signal from a second interconnect [new feedback path] [fig.2].
  - A phase locked loop [conventional PLL] receiving a reference clock signal [ref clock from input pin] and a delayed feedback clock signal [feedback signal from multiplexer is delayed by DL2], and supplying an output clock signal [signal from multiplexer] to said at least one driving circuit and said at least one receiving circuit, said phase locked loop generating said output clock signal according to said received reference clock signal and delayed feedback clock signal [fig.2; col.1, ll.56-64].
  - First and second delay elements [programmable delays DL1 and DL2] located in the path of said reference clock signal and the path of a feedback clock signal, respectively, said first and second delay element being configured to provide a delay in order to make said output signal meet a predetermined valid data timing requirement [via differential delay control scheme] [fig.2; col.3, ll.12-24, ll.30-39; col.3, l.64 – col.4, l.20].
7. As to claim 2, Sevalia discloses the delay elements [programmable delays DL1 and DL2] that are located only in the reference clock and feedback clock paths [fig.2].

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8. As to claim 3, Sevalia discloses the first and second delay elements that are self-calibrating delay cells [col.4, ll.5-17, ll.39-40, l.50; one time programming of estimated delay subsequently lets delay circuits to calibrate or tune accordingly to be in phase].

9. As to claims 4 and 19, Sevalia discloses the self-calibrating delay cells that calibrate themselves to meet specified timing adjustment, granularity and/or range [col.3, ll.40-63; col.4, ll.5-17, ll.39-40, l.50; transistors and other elements have rated performance specifications that are selected to be within a tolerable range for timing adjustment].

10. As to claims 5 and 20, Sevalia discloses the self-calibrating delay cells that use a digital compensation technique to reduce PVT variations [col.3, ll.52-59; col.4, ll.17-20, ll.45-54; configuration bits digitally set values to compensate for PVT variations, taking into account the PVT characteristics of the delay elements].

11. In re claim 18, Sevalia discloses a method of transferring a signal from a transmitting device [fig.2] to a receiving device [col.2, ll.19-25; circuit of fig.2 transmits clock signal to the device that the configurations are set to ensure timing is in phase] comprising:

- Outputting said signal from said transmitting device using a driving circuit [multiplexer] [col.3, l.10; col.4, ll.31-32].
- Receiving a reference clock signal in said transmitting device [fig.2; ref clock from input pin].
- Generating an output clock signal according to said received reference clock signal and a delayed feedback clock signal in a phase locked loop [conventional PLL; col.1, ll.56-64].
- Supplying the output clock signal [post divider clock signal] to said at least one driving circuit and at least one receiving circuit [feedback control switch] [fig.2].

- Providing a delay in a path of said reference clock signal and a path of said feedback clock signal [programmable delay DL1 and DL2] to make said at least one output signal meet a predetermined valid data timing requirement [col.3, ll.12-24, ll.30-39, l.64 -- col.4, l.27; output is in phase with input for data timing to be valid].

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia, in view of Roiter, US Patent 5636249.

14. In re claim 9, Sevalia and Roiter disclose each and every limitation of the claim as discussed above in reference to claim 1. In addition, Sevalia discloses an I/O circuit [col.1, ll.56-59] comprising:

- A transmitting device [fig.2] outputting at least one output signal [multiplexer outputs one signal], said transmitting device having:
  - At least one driving circuit [multiplexer], the number of driving circuits corresponding to the number of output signals [fig.2; col.3, l.10; col.4, ll.31-32].
  - A phase locked loop [conventional PLL] receiving a reference clock signal [ref clock from input pin] and a delayed feedback clock signal [feedback signal from multiplexer is delayed by DL2], said phase locked loop generating said output

clock signal according to said received reference clock signal and delayed feedback clock signal [fig.2; col.1, ll.56-64].

- First and second delay elements [programmable delays DL1 and DL2] located in the path of said reference clock signal and the path of a feedback clock signal, respectively, said second delay element to delay the feedback clock signal [fig.2; col.3, ll.12-24, ll.30-39; DL2 configured to provide a delay in order to make said output signal meet a predetermined valid data timing requirement], to determine whether an edge of the delayed feedback clock signal is early or late with respect to an edge of the feedback clock signal [col.2, l.45 – col.3, l.2; difference between an edge of input feedback signal into DL2 and a corresponding edge of output delayed feedback signal from DL2 constitutes the delay to be adjusted in order to provide a predictable input-output delay], and to increase or decrease the delay of the feedback clock signal based on whether an edge of the delayed feedback clock signal is early or late with respect to an edge of the feedback clock signal [col.4, ll.37-49; control DL2 accordingly to provide a predictable input-output delay].
- A receiving device having at least one receiving circuit [feedback control switch] receiving said at least one output signal from said transmitting device, and an input signal from an interconnect [control logic signal], said phase locked loop supplying an output clock signal [post divider clock signal] to said at least one driving circuit and said at least one receiving circuit, the timing of said received output clock signal or at least one output signal meeting said predetermined valid timing requirement [col.4, ll.17-20; configuration set up for device to get in phase signals in order to operate correctly].

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15. Sevalia did not discuss the details of the delay elements.
16. Roiter discloses a timing circuit [phase synchronization apparatus] comprising:
  - Delay elements [fig.2] to determine whether a rising edge of a signal [rds signal] is early or late with respect to a falling edge of a clock signal [bit rate clock] [fig.3; col.4, l.65 – col.5, l.29].
17. It would have been obvious to one of ordinary skill in the art, having the teachings of Sevalia and Roiter before him at the time the invention was made, to modify the timing circuit taught by Sevalia to include the teachings of Roiter [broad concept can be applied to all kinds of signals in general], in order to obtain the timing circuit comprising delay elements to determine whether a rising edge of the delayed feedback clock signal is early or late with respect to a falling edge of the feedback clock signal, and to increase or decrease the delay of the feedback clock signal based on whether the rising edge of the delayed feedback clock signal is early or late with respect to the falling edge of the feedback clock signal. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to align the edges of signals [Roiter: col.4, l.65 – col.5, l.29].
18. As to claim 10, Sevalia discloses the delay elements [programmable delays DL1 and DL2] that are located only in the reference clock and feedback clock paths [fig.2].
19. As to claim 11, Sevalia discloses the first and second delay elements that are self-calibrating delay cells [col.4, ll.5-17, ll.39-40, l.50; one time programming of estimated delay subsequently lets delay circuits to calibrate or tune accordingly to be in phase].
20. As to claim 12 and 19, Sevalia discloses the self-calibrating delay cells that calibrate themselves to meet specified timing adjustment, granularity and/or range [col.3, ll.40-63; col.4,

ll.5-17, ll.39-40, l.50; transistors and other elements have rated performance specifications that are selected to be within a tolerable range for timing adjustment].

21. As to claim 13 and 20, Sevalia discloses the self-calibrating delay cells that use a digital compensation technique to reduce PVT variations [col.3, ll.52-59; col.4, ll.17-20, ll.45-54; configuration bits digitally set values to compensate for PVT variations, taking into account the PVT characteristics of the delay elements].

22. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia as applied to claim 5 above, and further in view of Hamza, U.S. Patent 5818270.

23. Hamza was cited as prior art in the previous Office Action.

24. In re claim 6, Sevalia discloses every limitation of the claim as discussed above in reference to claim 5. Sevalia did not discuss utilizing a multi-tap delay buffer to delay a clock signal.

25. Hamza discloses a timing circuit [clock multiplier 10] that utilizes a multi-tap delay buffer [logical multiplier 14] in the clock signal [waveform 13] path to delay the clock signal, the amount of delay being controlled by selecting a tap of the multi-tap delay buffer [col.2, ll.41-60].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Sevalia and Hamza before him at the time the invention was made, to modify the timing circuit taught by Sevalia to include the multi-tap delay buffer as taught by Hamza, in order to obtain the timing circuit wherein the digital compensation technique utilizes a multi-tap delay buffer in the feedback clock signal path to delay the feedback clock signal with the amount of delay being controlled by selecting a tap of the multi-tap delay buffer. One of ordinary skill in the art would

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have been motivated to make such a combination as it provides a way to contribute to the reduction of power and PVT variations [particularly the temperature] [Hamza: col.1, ll.37-39].

27. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia and Roiter as applied to claim 1 above, and further in view of Byrn et al., U.S. Patent 5977837, hereinafter Byrn.

28. Byrn was cited as prior art in the previous Office Action.

29. In re claim 7, Sevalia discloses every limitation of the claim as discussed above in reference to claim 1. Sevalia did not discuss the timing circuit comprising a plurality of driving circuits.

30. Byrn discloses a timing circuit [phase selector circuit 200] comprising a plurality of driving circuits [external frequency dividers 204, 206, and 208] and a phase locked loop [202] providing an output clock signal [PLL out] to all of the plurality of driving circuits [fig.2; col.2, ll.54-62].

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Savalia and Byrn before him at the time the invention was made, to modify the timing circuit taught by Sevalia to include the plurality of driving circuits as taught by Byrn, in order to obtain the timing circuit with the plurality of driving circuits for outputting a plurality of clock signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to output a plurality of clock signals.

32. As to claim 8, Byrn discloses the plurality of driving circuits that drive respective output signals from an IC chip [CMOS microprocessor] [col.1, ll.15-18; external is relative to the synchronization path].

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33. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia and Roiter as applied to claim 13 above, and further in view of Hamza as applied to claim 6 above.

34. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia and Roiter as applied to claim 9 above, and further in view of Byrn as applied to claim 7 above.

35. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia and Roiter as applied to claim 9 above, and further in view of Goldrian, U.S. Patent 5742798.

36. Goldrian was cited as prior art in the previous Office Action.

37. In re claim 16, Sevalia and Roiter disclose every limitation of the claim as discussed above in reference to claim 9. Sevalia and Roiter did not disclose expressly the I/O circuit operating with a bus.

38. Goldrian discloses an I/O circuit [fig.2] wherein the transmitting device [clock generator 200] and the receiving device [chip-A 204] comprise IC chips and the output signals [201] are driven on a bus [bus comprises of lines 201-203] between the IC chips [col.3, ll.27-54].

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Sevalia, Roiter and Goldrian before him at the time the invention was made, to use the IC chip-bus setting as taught by Goldrian for the I/O circuit disclosed by Sevalia and Roiter as the setting taught by Goldrian is suitable for use with the I/O circuit of Sevalia and Roiter. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase processing efficiency [col.1, ll.14-28].

40. As to claim 17, Goldrian discloses the transmitting device and the receiving device are mounted at a distance from each other on a printed circuit board [col.1, l.11].

*Response to Arguments*

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41. Applicant's arguments dated May 19, 2006 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen  
June 22, 2006

  
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